AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the above-referenced application.

Listing of Claims:

Claims 1-14 (Cancelled)

15. (Previously presented) A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising:

an inverter chain containing not less than four inverters;

a p-channel metal-oxide-semiconductor transistor and an n-channel metal-oxide-semiconductor transistor, known as MOS transistors, to comprise each of the at least four inverters, wherein a gate threshold voltage of each gate is shifted in mutually opposing directions;

low threshold voltage n-MOS transistors of each of a first and a third inverter connected to ground by a high threshold voltage n-MOS transistor; and

low threshold voltage p-MOS transistors of each of a second and a fourth inverter connected to ground by a high threshold voltage p-MOS transistor;

wherein, when an input logic signal is fixed at a low level during a standby state, said high threshold voltage n-MOS transistor is set to an off-state in response to a chip select signal controlling said standby state, and said high threshold voltage p-MOS transistor is set to an off-state in response to said chip select signal that is negated.

Claims 16-18 (Cancelled)

19. (Previously presented) A delay circuit, comprising:

first and second nodes;

a first inverter, the output of which coupled to said first node, said first inverter receiving a logic signal;

a second inverter, the input of which coupled to said first node and the output of which coupled to said second node;

a first capacitor coupled between said first node and a first power source line, said first capacitor being a first transistor of a first channel type; and

a second capacitor coupled between said second node and a second power source line which is different from said first power source line, said second capacitor being a second transistor of a second channel type which is different from said first channel type,

wherein, when the logic signal is fixed at a low level during a standby state, one of said first capacitor and said second capacitor is set to an off-state in response to a chip select signal controlling said standby state, and the other of said first capacitor and said second capacitor is set to an off-state in response to said chip select signal that is negated.

20. (Previously presented) A delay circuit, comprising:

first and second nodes;

a first inverter, the output of which coupled to said first node, said first inverter receiving a logic signal;

a second inverter, the input of which coupled to said first node and the output of which coupled to said second node;

a first capacitor coupled between said first node and a first power source line, said first capacitor being a first transistor of a first channel type; and

a second capacitor coupled between said second node and a second power source line which is different from said first power source line, said second capacitor being a second transistor of a second channel type which is different from said first channel type; wherein said first transistor is a p-MOS transistor, said second transistor is an n-MOS transistor, and said second power source line is fixed at a ground potential.

21. (Previously presented) A delay circuit according to claim 19, wherein said first transistor is an n-MOS transistor, said second transistor is a p-MOS transistor, and said first power source line is fixed at a ground potential.

22. (Previously presented) A delay circuit, comprising:

first, second and third nodes;

a first inverter, the output of which coupled to said first node, said first inverter receiving a logic signal;

a second inverter, the input of which coupled to said first node and the output of which coupled to said second node;

a third inverter, the input of which coupled to said second node and the output of which coupled to said third node;

a fourth inverter, the input of which coupled to said third node;

a first capacitor coupled between said first node and a first power source line, said first capacitor being a first transistor of a first channel type;

a second capacitor coupled between said third node and said first power source line, said second capacitor being a second transistor of said first channel type; and

wherein no capacitor is connected to said second node

23. (Previously presented) A delay circuit according to claim 22, wherein said first transistor and said second transistor are p-MOS transistors, and said first power source line is fixed at a power potential.

24. (Previously presented) A delay circuit according to claim 22, wherein said first transistor and said second transistor are n-MOS transistors, and said first power source line is fixed at a ground potential.

Claims 25 - 26 (Cancelled)

27. (Previously presented) A delay circuit receiving a logic signal having a first logical level and a second logical level, comprising:

an inverter chain including a plurality of inverters and at least one first capacitor, said inverter chain receiving said logic signal,

said first capacitor including a MOS transistor of a first channel type,

said first capacitor being operated so that the capacitor changes in off-state to on-state to increase its capacitance when said logic signal changes from said first logical level to said second logical level, whereby said inverter chain outputs a first delay signal generated after a first delay time from the transition timing from said first to said second logical levels of said logic signal,

said first capacitor being operated so that the capacitor changes in said on-state to said off-state to decrease its capacitance when said logic signal changes from said second logical level to said first logical level, whereby said inverter chain outputs a second delay signal generated after a second delay time from the transition timing from said second to said first logical levels of said logic signal, said second delay time being shorter than said first delay time,

a logical gate receiving the output of said inverter chain and said logic signal so that said logical gate outputs its output signal in response to said first delay signal when said logic signal changes from said first logical level to said second logical level.

28. (Previously presented) A delay circuit according to claim 27, further comprising:

a second capacitor,

said second capacitor being comprised of an MOS transistor of a second channel type which is different from said first channel type,

said second capacitor being coupled to a node which is different from the node coupled to said first capacitor in said inverter chain,

said second capacitor being operated so that the capacitor changes in off-state to on-state to increase its capacitance when said logic signal changes from said first logical level to said second logical level, whereby said inverter chain outputs a first delay signal generated after a first delay time from the transition timing from said first to said second logical levels of said logic signal,

said second capacitor being operated so that the capacitor changes in said on-state to said off-state to decrease its capacitance when said logic signal changes from said second logical level to said first logical level, whereby said inverter chain outputs a second delay signal generated after a second delay time from the transition timing from said second to said first logical levels of said logic signal, said second delay time being shorter than said first delay time.

29. (Currently amended) A delay circuit, comprising:

2n+1 nodes defined in series, n being a natural number, a first node receiving a logical signal;

2n inverters, each inverter arranged between adjacent nodes of said 2n+1 nodes;

a capacitor of an n-MOS type coupled between an [[odd]] even node and a power source line; and

a NOR gate coupled to the first node and the [[2n-th]] (2n+1)th node.

30. (Currently amended) A delay circuit, comprising:

2n+1 nodes defined in series, n being a natural number, a first node receiving a logical signal;

2n inverters, each inverter arranged between adjacent nodes of said 2n+1 nodes;

a capacitor of an n-MOS type coupled between an [[even]] odd node and a first power source line;

a capacitor of a p-MOS type coupled between an [[odd]] even node and a second power source line; and

an AND gate coupled to the first node and the [[2n-th]] (2n+1)th node.

31. (Currently amended) A delay circuit, comprising:

2n+1 nodes defined in series, n being a natural number, a first node receiving a logical signal;

2n inverters, each inverter arranged between adjacent nodes of said 2n+1 nodes;

a capacitor of an n-MOS type coupled between an [[even]] odd node and a first power source line;

a capacitor of a p-MOS type coupled between an [[odd]] even node and a second power source line; and

a NAND gate coupled between the first node and the [[2n-th]] (2n+1)th node.